ABSTRACT OF THE DISCLOSURE

A contact structure for a ferroelectric memory device integrated in a semiconductor substrate and includes an appropriate control circuitry and a matrix array of ferroelectric memory cells, wherein each cell includes a MOS device connected to a ferroelectric capacitor. The MOS device has first and second conduction terminals and is covered with an insulating layer. The ferroelectric capacitor has a lower plate formed on the insulating layer above the first conduction terminals and connected electrically to the first conduction terminals, which lower plate is covered with a layer of a ferroelectric material and coupled capacitively to an upper plate. Advantageously, the contact structure comprises a plurality of plugs filled with a non-conductive material between the first conduction terminals and the ferroelectric capacitor, and comprises a plurality of plugs filled with a conductive material and coupled to the second conduction terminals or the control circuitry.

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